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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/988,272	11/19/2001	Hirotooshi Kubo	981206A	8401

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ARMSTRONG, WESTERMAN & HATTORI, LLP
1725 K STREET, NW
SUITE 1000
WASHINGTON, DC 20006

EXAMINER

HOGANS, DAVID L

ART UNIT PAPER NUMBER

2813

DATE MAILED: 08/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary

Application No.

09/988,272

Applicant(s)

KUBO ET AL.

Examiner

David L. Hogans

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 July 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 12-15, 22 and 23 is/are pending in the application.
- 4a) Of the above claim(s) 16-21 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 12-15, 22 and 23 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 November 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Election filed on July 1, 2003.

Election/Restrictions

1. Applicant's election without traverse of Claims 12-15 and 22-23 in Paper No. 5 is acknowledged.
2. Claims 16-21 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 5.

Drawings

1. Figures 19-26 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

Priority

2. Applicant has not complied with one or more conditions for receiving the benefit of an earlier filing date (noting section 16a of Applicant's Utility Patent Application Transmittal form) under 35 U.S.C. §120 as follows:

An application in which the benefits of an earlier application are desired must contain a specific reference to the prior application(s) in the first sentence of the specification or in an application data sheet (37 CFR 1.78(a)(2) and (a)(5)). The specific reference to any prior nonprovisional application must include the relationship (i.e., continuation, divisional, or continuation-in-part) between the applications except when the reference is to a prior application of a CPA assigned the same application number.

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3. Acknowledgment is made of applicant's claim for priority under 35 U.S.C. 119(a)-(d) based upon an application filed in Japan on August 8, 1997 (noting Applicant's Utility Patent Application Transmittal form). A claim for priority under 35 U.S.C. 119(a)-(d) cannot be based on said application, since the United States application was filed more than twelve months thereafter. **Status of Claims**

Claims 12-15 and 22-23 are pending. Claims 16-21 are withdrawn from further consideration.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claim 15 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The specification fails to elucidate patterning the fourth thick insulating layer so as to remain a peripheral region of the substrate, prior to forming the drain region.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

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invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 12-14 and 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over 4,879,254 to Tsuzuki et al in view of 5,879,968 to Kinzer.

Claim 12

Tsuzuki et al. teaches a method of fabricating a semiconductor device, comprising the steps of: forming a drain layer (2) of a first conduction type on a surface of a semiconductor substrate (1) of the first conduction type; forming a first insulating film (3) on said drain layer (2); forming a first conductive layer (4) on said first insulating film (3); forming a second insulating film (5) on said first conductive layer (4); patterning said second insulating film, said first conductive layer, and said first insulating film, to form a gate insulating film (3) from said first insulating film, and a gate electrode (4) from said first conductive layer; implanting an impurity of a second conduction type (7) opposite to the first conduction type into a surface of said drain layer with using said gate electrode as a mask, thereby forming a channel region of the second conduction type (7); implanting an impurity of the first conduction type (8) into said channel region with using said gate electrode as a mask, thereby forming an impurity region of the first conduction type (8); forming a third insulating film (9) so as to cover a surface of the impurity region, side walls of said gate insulating film, said gate electrode, and said second insulating film, and an upper face of said second insulating film; etching back said third insulating film to form a side wall insulator (9a) of said third insulating film, by remaining said third insulating film selectively on side walls of said gate insulating film,

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said gate electrode, and said second insulating film; etching the impurity region to form a recess (10) so as to penetrate the impurity region, thereby forming a source region (8) of the impurity region; and forming a second conductive layer (11) on an entire surface, and patterning said second conductive layer, thereby forming a wiring layer. (See Figures 1, 4 and 7 and columns 3-4 lines 35-54, column 5 lines 35-63, column 7 lines 12-58)

Tsuzuki et al. fails to explicitly teach forming the sidewall insulator on the side walls of the gate insulating film and patterning the metal layer.

However, Kinzer, in Figures 1-5 and columns 3-5 lines 01-15, teaches etching through the gate oxide (31) and then forming an insulation layer (60) over the sidewalls of the gate oxide (31) and patterning the metal layer.

It would have been obvious to one of ordinary skill in the art to modify Tsuzuki et al. by incorporating etching through the gate oxide so that an insulation layer could be placed over the sidewalls of the gate oxide and patterning the metal layer, as taught by Kinzer, to reduce the amount of energy needed when performing subsequent implant steps (i.e. - subsequent implantations need not penetrate the gate oxide layer) and to form a metal wiring layer that selectively interconnects contacts.

Additionally, the Examiner notes that the specification contains no disclosure of either the critical nature of the claimed processes or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen processes or upon another variable recited in a claim, the Applicant must show that the chosen processes are critical. *In re Woodruff*, 919 F.2d 1575, 1578 (Fed. Cir. 1990)

Claim 13

Incorporating all arguments of Claim 12 and noting that Tsuzuki et al. teaches introducing an impurity of the second conduction type into the bottom of the recess to form a body contact region of the second conduction after etching the impurity region prior to forming a second conductive layer. (See Figures 1, 4 and 7 and columns 3-4 lines 35-54, column 5 lines 35-63, column 7 lines 12-58)

Claim 14

Incorporating all arguments of Claim 12 and noting that Tsuzuki et al. fails to explicitly teach wherein the etching step comprises the steps of: forming a mask pattern having an opening located in a center of the impurity region and cover an entire surface except for the opening before etching the impurity region; etching the impurity region by using the mask pattern to form a recess deeper than the impurity region, thereby forming a source region of the impurity region remained; and introducing an impurity of the second conduction type into the bottom of the recess to form a body contact region of the second conduction type.

However, Kinzer, in Figures 1-5 and columns 3-5 lines 01-15, teaches forming a mask pattern (61) having an opening located in a center of the impurity region (50 or 51) and cover an entire surface except for the opening before etching the impurity region; etching the impurity region by using the mask pattern (61) to form a recess (70 or 71) deeper than the impurity region (50 or 51), thereby forming a source region (50 or 51) of the impurity region remained; and introducing an impurity of the second conduction type (75 or 76) into the bottom of the recess to form a body contact region (75 or 76) of the second conduction type.

It would have been obvious to one of ordinary skill in the art to modify Tsuzuki et al. by incorporating a mask pattern to etch a recess deeper than the impurity region and then introduce another impurity into the bottom of the recess, as taught by Kinzer, to form well aligned base regions that are located at the axis of each of the individual cells.

Claim 22

Incorporating all arguments of Claim 12 and noting that Tsuzuki et al. teaches wherein an upper surface and a side surface of the source region are directly contacted with the wiring layer. (See Figures 1, 4 and 7 and columns 3-4 lines 35-54, column 5 lines 35-63, column 7 lines 12-58)

Claim 23

Incorporating all arguments of Claim 14 and noting that Kinzer teaches wherein the opening of the mask pattern is formed smaller than a region of the impurity region between the adjacent sidewall insulators. (See Figures 1-5 and columns 3-5 lines 01-15)

It would have been obvious to one of ordinary skill in the art to modify Tsuzuki et al. by incorporating an opening of the mask pattern that is formed smaller than a region of the impurity region between the adjacent sidewall insulators, as taught by Kinzer, to create source/drain regions adjacent to each gate electrode that can be contacted with the metal layer to make the intentional short between the source/drain regions and the body contact.

8. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over 4,879,254 to Tsuzuki et al in view of 5,879,968 to Kinzer in view of Applicant's Admitted Prior Art.

Incorporating all arguments of Claim 12 and noting that Tsuzuki et al. and Kinzer fail to explicitly teach a fourth insulating layer formed on the substrate that is patterned so as to remain a peripheral region on the substrate.

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However, Applicant's specification, page 2 lines 10-18, discloses a thick oxide that is patterned to be formed in bonding pad site regions (i.e. – on the periphery of the substrate).

It would have been obvious to one of ordinary skill in the art to modify Tsuzuki et al. and Kinzer by incorporating a fourth insulating layer formed on the substrate that is patterned so as to remain a peripheral region on the substrate, as taught by Applicant's Admitted Prior Art, to create regions for bonding pads.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David L. Hogans whose telephone number is (703) 305-3361. The examiner can normally be reached on M-F (7:30-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on (703) 308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.


CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

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July 22, 2003